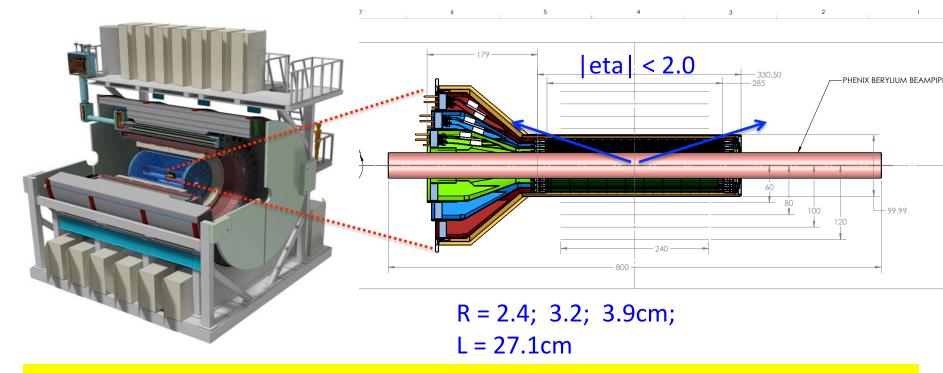
MVTX Status and Plan

Ming Liu Los Alamos

MAPS-based Vertex Detector (MVTX)



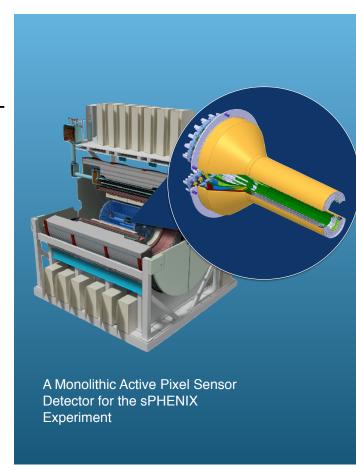
- "Adopt" ALICE ITS Upgrade Inner Barrel 3-layer MAPS detector
 - Mini. risk, Max. Physics
- Precision vertexing for b-jet/B-hadron tagging with high efficiency and high purity
- B-jet modification in QGP at low-medium pT to determine QGP properties, study massdependence on collisional vs radiative energy loss, flow etc.
- A separate DOE MIE to build the full detector, WBS 1.12, ~\$5M for construction;
- Early R&D by LANL LDRD, \$5M, FY17-19, readout and mechanical integration;

Outline

- MVTX Pre-proposal
- BNL Director's review
- R&D status and plan
 - Stave
 - Readout
 - PS and Controls
 - MOSAIC test bench
- Mechanical integration
 - MVTX/INTT/TPC

MVTX Pre-proposal Submitted!

- Pre-proposal submitted to DOE, 2/2017
 - Follow-up discussions with DOE and BNL managers
 - Weekly proj. leaders meeting BNL/LANL/LBNL/MIT
- Plan to update proposal to DOE, late 2017
 - Expanded science "CD0" + Cost & Schedule "CD1"
 - Funding in FY18, stave production @CERN in Aug.
 2018+, ~6 months;
 - Other options being explored for stave production @CERN/CCNU for delayed funding
- BNL Director's Review: July 10-11, 2017
 - Expand science case, "CD0"
 - Update Cost & Schedule, "CD1"
 - A dry run next Monday 6/19



A growing collaboration!

new sPHENIX/MVTX members:

- Czech groups
- CCNU lab
- USTC
- Peking Univ.

A great opportunity for:

- Physics
- Detector R&D
- Hardware
- Offline software

7 Organization and Collaboration

Here we discuss the current collaborating institutions and their focus areas. Based on their technical expertise and available resources, LANL, LBNL and MIT/Bates groups are leading the three major technical tasks of the project: 1) readout electronics integration; 2)carbon mechanical support frames production and 3) cooling and mechanical system integration, respectively.

Los Alamos National Lab (LANL): Readout electronics and mechanics integration.

Lawrence Berkeley National Lab (LBNL): Carbon structure, production, LV and HV power system, full detector assembly and test.

Brookhaven National Lab (BNL): System integration and services, safety and monitoring.

Massachusetts Institute of Technology (MIT/Bates): Mechanical system integration and cooling.

Massachusetts Institute of Technology (MIT): Stave assembly and testing at CERN.

University of Texas at Austin (UT Austin): MVTX readout electronics integration and testing.

University of Colorado: b-jet simulations and future hardware.

Iowa State University (ISU): Detector assembly and testing, simulations.

Florida State University (FSU): Offline and simulations.

University of New Mexico (UNM): LV cabling & connectors.

New Mexico State University (NMSU): Tracking algorithm and physics simulations.

Georgia State University (GSU): Online software and trigger development.

University of California at Los Angeles (UCLA): Simulation and readout testing.

University of California at Riverside (UCR): Detector assembly and testing, simulations.

Yonsei University (Korea): MAPS chips QA and readout, simulations

RIKEN/RBRC (Japan): Mechanical integration, cooling, cabling, simulation, patter recognition.

Purdue: Detector assembly and testing, analysis. Silicon lab available.

Central China Normal University (CCNU/China): MAPS chip and stave test at CERN and/or CCNU.

Univ. of Science and Technology of China (USTC/China): MAPS chip and stave test, simulations.

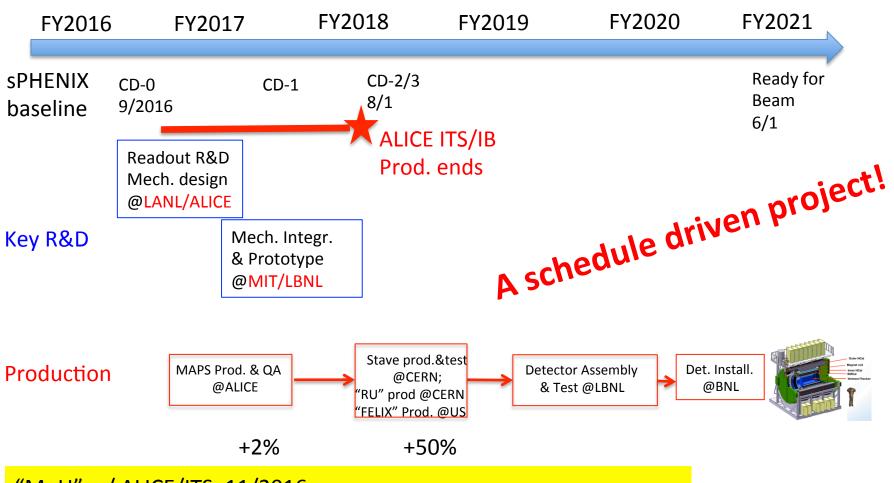
Scope of the MVTX Project

- MAPS staves & Electronics
 - MAPS Detectors
 - "MoU" to build 68 ITS MAPS staves
 - No modification
 - Readout Electronics
 - Frontend: ALICE/ITS, RU
 - Backend: ATLAS FELIX
 - Modify/reprogram RU & FELIX for sPHENIX
 - R&D by LANL LDRD
 - Production
 - Extend ALICE/ITS MAPS stave production
 - sPHENIX personnel help assembly and testing staves at CERN
 - Reproduce additional ALICE RU & FELIX for sPHENIX
 - Final assembly and test in US, LBNL/BNL
 - Ancillary systems, copy ALICE
 - LV/HV, cables, crates, racks etc.
 - Slow control, safety and monitoring

- Mechanics & Cooling
 - No/(some) changes to ALICE/ITS inner tracker mechanical structures
 - End Wheels
 - Cylindrical structure shells
 - Detector half barrels
 - Detector and Service half barrels
 - Mechanical Integration
 - Conceptual design by LANL LDRD
 - Prototype by sPHENIX R&D
 - Design integration frames
 - · Carbon frames etc.
 - Installation tooling etc.
 - Copy ALICE cooling plant design
 - Minor modification to fit sPHENIX
 - Smaller heat load than ALICE ITS
 - Metrology and Survey

WBS 1.12: a new MIE fund the full MAPS Vertex Detector, ~\$5M

Project Tasks and Timeline



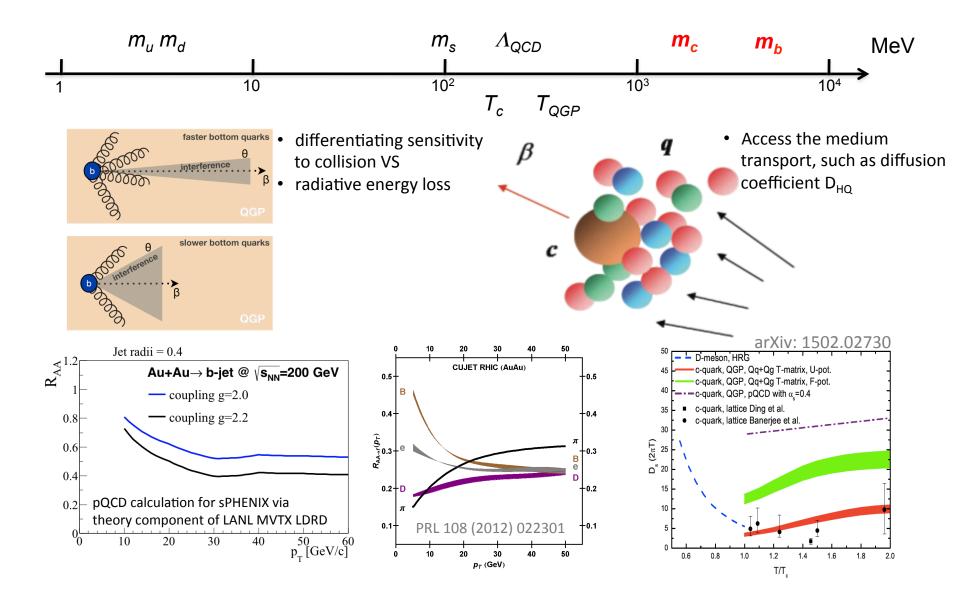
"MoU" w/ ALICE/ITS: 11/2016

- Produce MAPS chips and Stave Space frames for sPHENIX as part of ALICE production!
- Full staves and RU & CRU production cost & schedule → MVTX MIE

Prepare for the BNL Director's Review

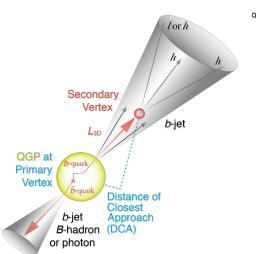
- Science
 - HF-Jet Topical Group Preliminary for a dry run next week
 - B hadron physics
 - B-jet physics
 - Detector performance plots
 - Near final "money plots" for July review
- Cost and Schedule
 - Updated WBS structure and org chart
 - Work in progress, cost & schedule, 6/5/2017
- MVTX stave production options
 - Ming's visit to CCNU in May
 - Maria's visit to CERN this week

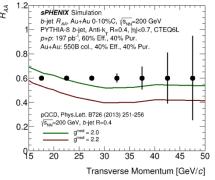
Uniqueness of Heavy Quarks in QCD

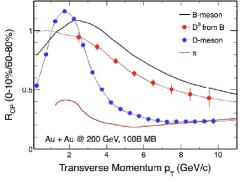


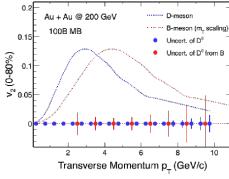
HF-topical group

- HF in sPHENIX: in particular B-meson and b-jets, provide differentiating sensitivity to collision VS radiative energy loss, access to HQ transport parameter of QGP, total cross section. Bring results to precision era.
 - O<p_T<15 GeV/c B-meson: access down to zero pT, max sensitivity to HQ mass effect
 - p_T>15 GeV/c b-Jet: less dependence on FF complication, probing parton kinematics and higher p_T-scale
- High priority task are set to develop and simulate performance for coming MVTX reviews and proposals, expanding the program in HF-jet and HF-meson programs









Communication:

- Discussion email list: https://lists.bnl.gov/mailman/listinfo/sphenix-hf-jets-l
- Wiki page under construction: https://wiki.bnl.gov/sPHENIX/index.php/Heavy-Flavor-Topical Group

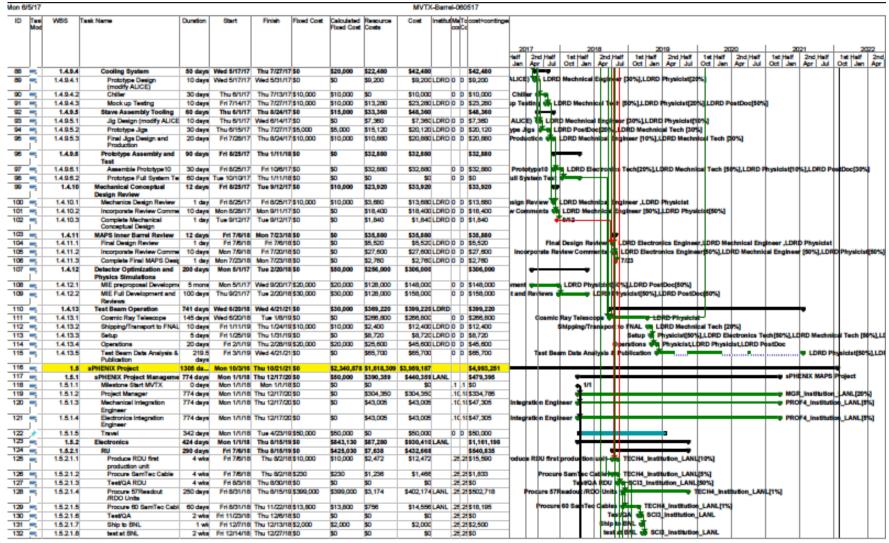
Meetings/Events

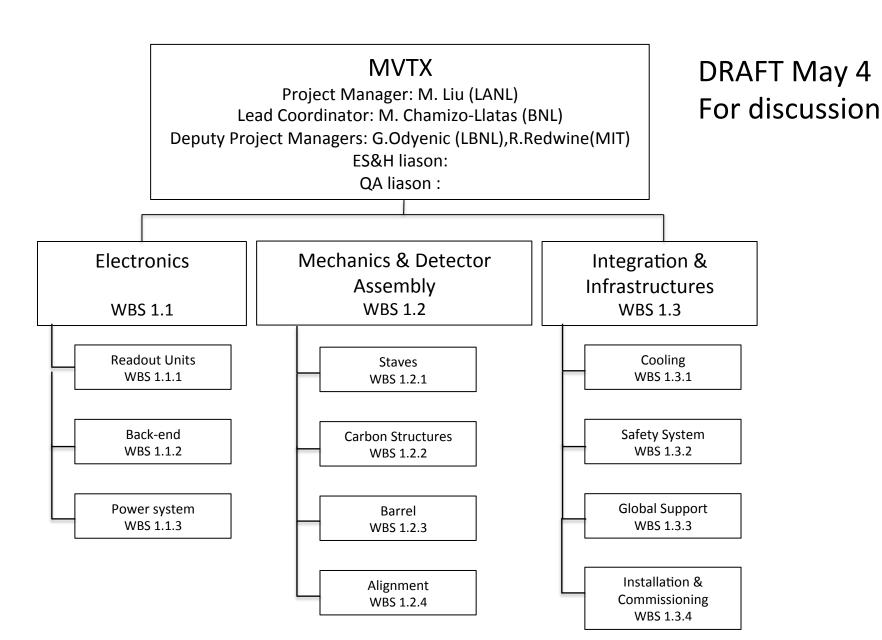
- Use weekly simulation meetings for updates, https://indico.bnl.gov/categoryDisplay.py?categId=88
- Monthly TG meetings: https://indico.bnl.gov/categoryDisplay.py?categId=151
- Goal oriented irregular events:

MVTX brainstorming meeting, Mar 8 / MAPS+HF-jet joint workfests, e.g. Jan 5-7 2017 @ Santa Fe / Precollaboration meeting work-fest on May 16-17, 2016 / Initial TG meeting on Apr 22, 2016

Updated Cost and Schedule WBS: 6/5/2017

Dave Lee et al





MVTX R&D Status and Plan

Readout R&D

- 5 single-chip MAPS tested at LANL
- Workfest @UT-Austin, 4/19-20
- RUv1 available in July, will be used for LDRD telescope
- BNL/ATLAS FELIX being evaluated as the default backend
 - Computer arrived, fibers/cables ordered
 - Obtain one FELIX in a few weeks
 - "CRU" being prototyped with Altera evaluation boards, able to communicate with the RUv0 board @ UT-Austin;
- LANL MOSAIC test bench in operation!

Tracker integration task force

- MVTX + INTT + TPC mechanical system integration
- Identified the major tasks

Stave production @CERN

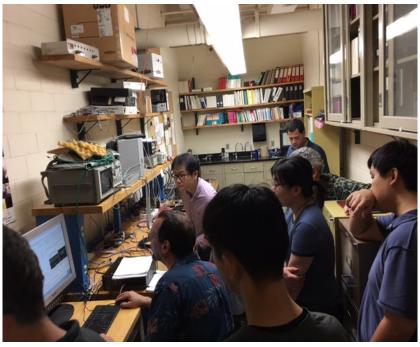
- ALICE Stave Production Readiness Review 4/27, prod. Starts in June/July
- LANL people do assembly and testing at CERN, May Sept. 2017
- MVTX plan

MVTX Readout Workfest @UT-Austin, 4/19-20

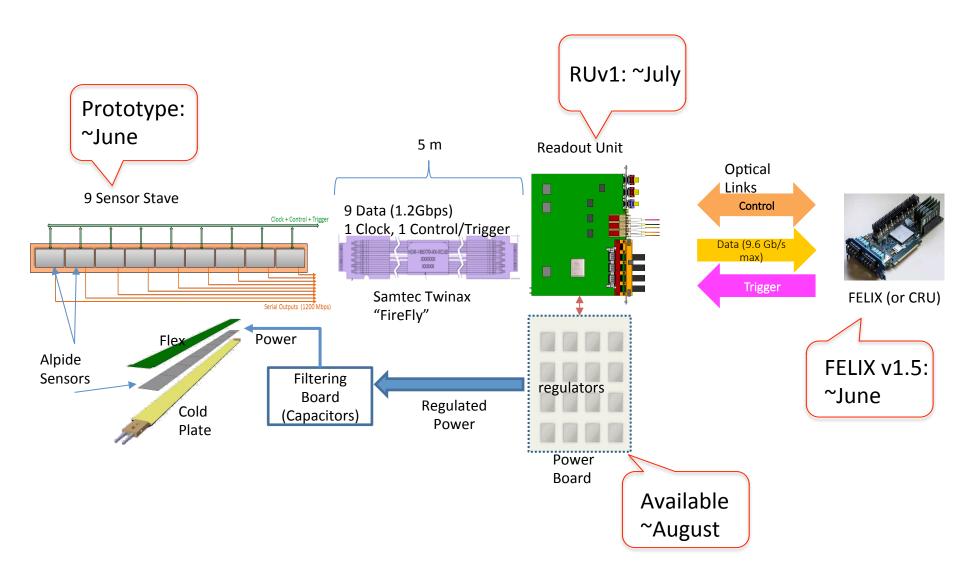
https://indico.bnl.gov/conferenceDisplay.py?confld=3047

- Very productive discussions:
 - sPHENIX readout Martin
 - TPC readout Jin and Takao
 - ALICE ITS readout system Jo
 - LV/HV and Slow controls Giacomo
 - MVTX readout options Mark
- Lab demo of RUv0 and "CRU" R&D
 - -RUv0
 - "CRU" prototype with an Altera eval. board
- A brief summary
 - Defined a possible MVTX readout path
 - RDO Unit, some modification
 - · CRU/FELIX (TPC), significant R&D needed
 - Joint R&D on RU and CRU, maybe also FELIX integration
 - UT-Austin's interest in RU and CRU production & test!





MVTX Readout and Control System Status

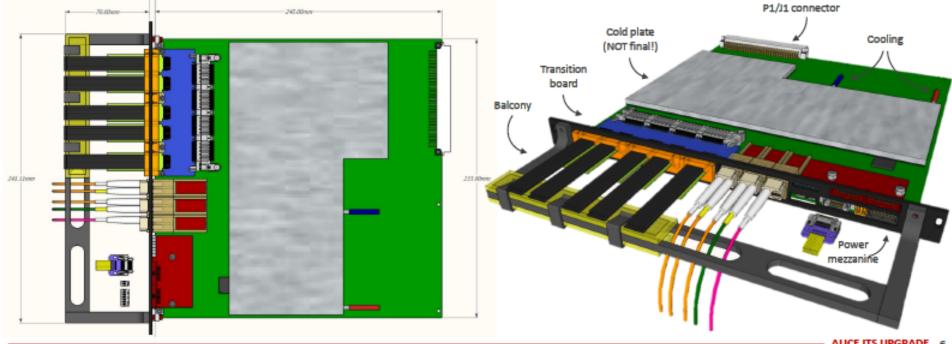


ALICE/ITS Readout R&D

5 RUv1 available for LANL R&D ~July 2017

RUv1 – Overview (board general layout an connectors fixed)

- All connectors fixed (connectors toward Power Units mounted on mezzanine, upgradable).
- PCB size $233 \times 240 \text{ mm}^2$, VME slot compliant, VME J1 for power/ground. (1 1.5 kg cold plate included).
- ITS crates will accommodate 340mm deep Power Boards, a passive extender is envisaged.
- P1/J1 positioning makes the RUv1 vertical orientation FIXED (data connectors on top)
- Critical: data cable connector length (Antoine design) vs balcony depth (70mm now)
- Critical: check power board volume compatibility (few mm available on top side of RUv1 in case)



Electronics R&D - Cont.

FELIX and MVTX Power Distribution Boards

FELIX: visited BNL Labs and had FELIX system demo

- V1.5 boards, all functionalities available- data, slow control and Timing/Trigger/Busy, w/ GBT
- Multi-channel GBT links and PCIe interface code developed, with examples of user modules
- V2.0, available ~end of 2017, sPHENIX application
- A 1.5v FELIX board produced and tested, ready for shipment to LANL; Optical cables etc. to be ordered soon for LANL test bench

Power distribution boards and PS

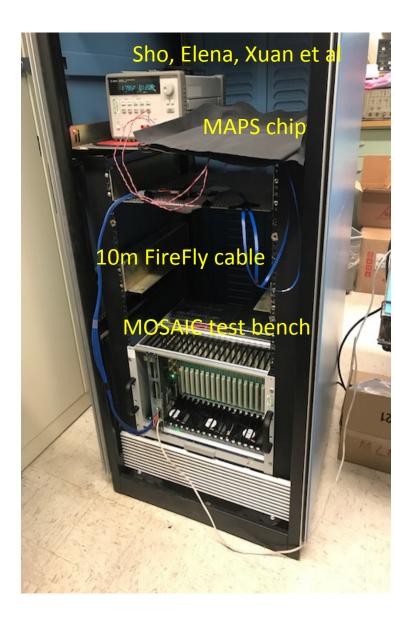
- LBNL PS distribution board available for R&D from CERN/ LBNL ~ August. Order placed, 4wks + testing
- R&D power supply and control system ordered (CAEN), available ~August





R&D @LANL on MAPS Single Chip Readout

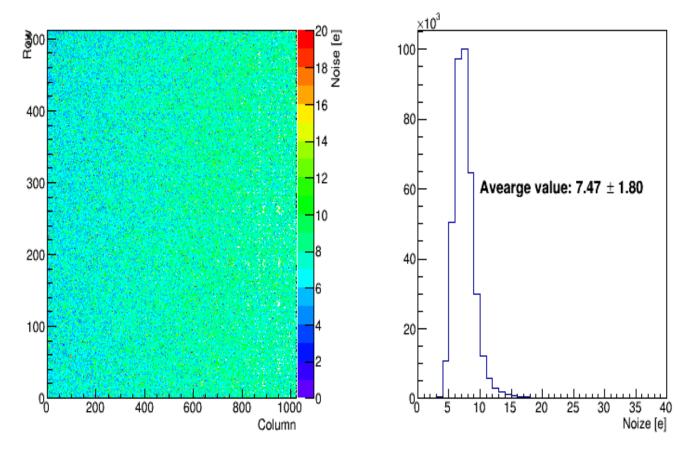
- MOSAIC test bench in operation
 - Single MAPS chip with high-speed readout
 - Threshold scan
 - Noise scan
 - External trigger
 - Test data readout performance
 - 1.2Gb/sec
 - 0.6Gb/sec
 - 0.4Gb/sec
- Test firefly cable performance
 - 5m (ALICE default)
 - 7m, 10m
 - Short extension cables, +20~30cm



Test under internal trigger (40MHz)

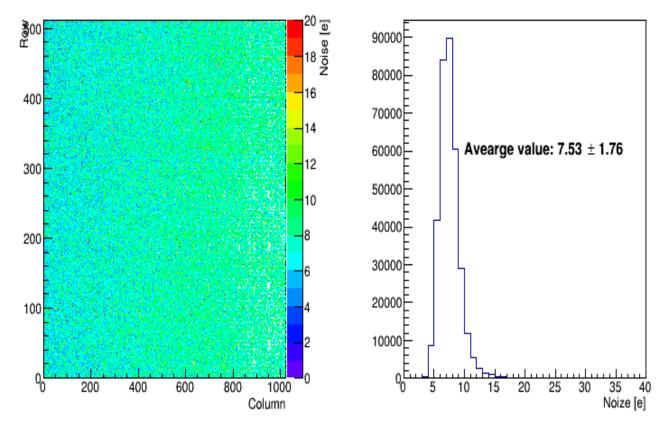
From Xuan

- Readout speed 1.2 Gb/s and 50 injections.
- Scan the noise per pixel and the average value is 7.47±1.80 (e).



Test under internal trigger (40MHz)

- Readout speed 600 Mb/s and 50 injections.
- Scan the noise per pixel and the average value is 7.53±1.76 (e).



External Trigger and Source

Single chip readout

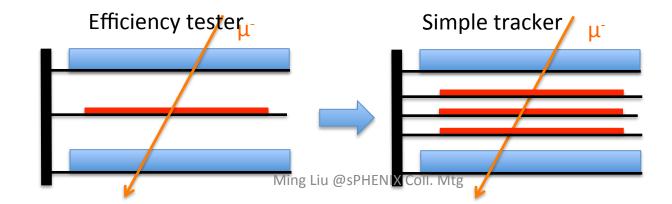
 Use a pulse generator as the external trigger

- Use the Strontium-90 to produce beta rays.
 - Vary the distance between the source and the silicon chip



A Single-chip MAPS Telescope

- Check the readout occupancy and efficiency under different internal trigger clock (10-40MHz), readout speed (400-1200Mb/s) and threshold (set up by the analog signal or the configuration file?).
- Set cosmic ray triggers with scintillator bars or pads to read out single MVTX chip with the external coincidence cosmic ray trigger.
- Design of single chip based telescope in progress

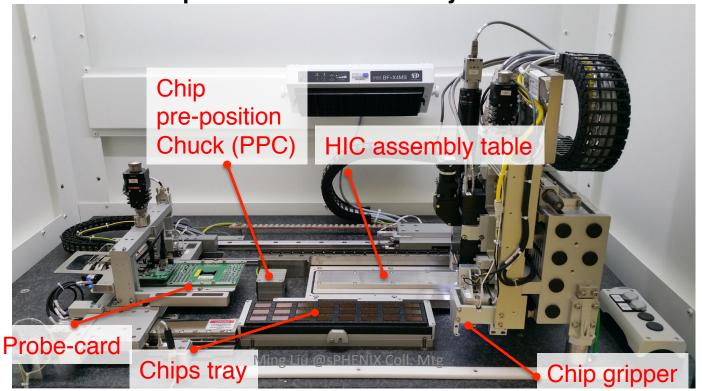


Stave Production & Test @ CERN

From Sanghoon

- Under preparation for massive stave production
 - Overall ALPIDE chip test and HIC/stave production procedure is well established Successful ITS Stave production readiness review on Apr/27
 - Optimization of fine configuration is underway
 - Expect to finalize the entire procedure with a new set of ALPIDE chips w/o PIQ which will be ready soon
 - ALPIDE chips with PIQ will be available from mid July

Chip test and HIC assembly machine

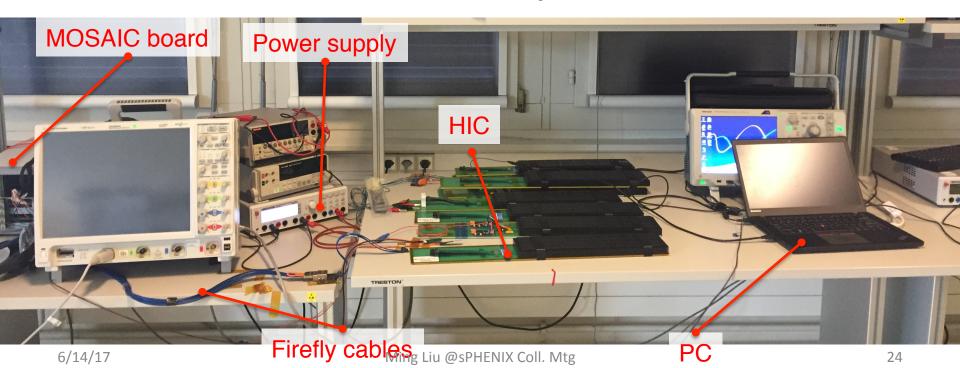


Stave Production & Test @ CERN

- Prototype HICs and staves will be available for LANL R&D soon
 - Multichip readout
 - Mechanical cooling

Sanghoon, Cesar et. al. working @CERN May – Sept. 2016
Czech group – postdocs + Tech @CERN

HIC/Stave test setup @CERN



MVTX Stave Production Plans

- Plan-A
 - CERN production:
 - Assembly and test
 - Time: starting 08/2018, 6-9 months

DOE Budget: FY18

Impact on sPHENIX start date?

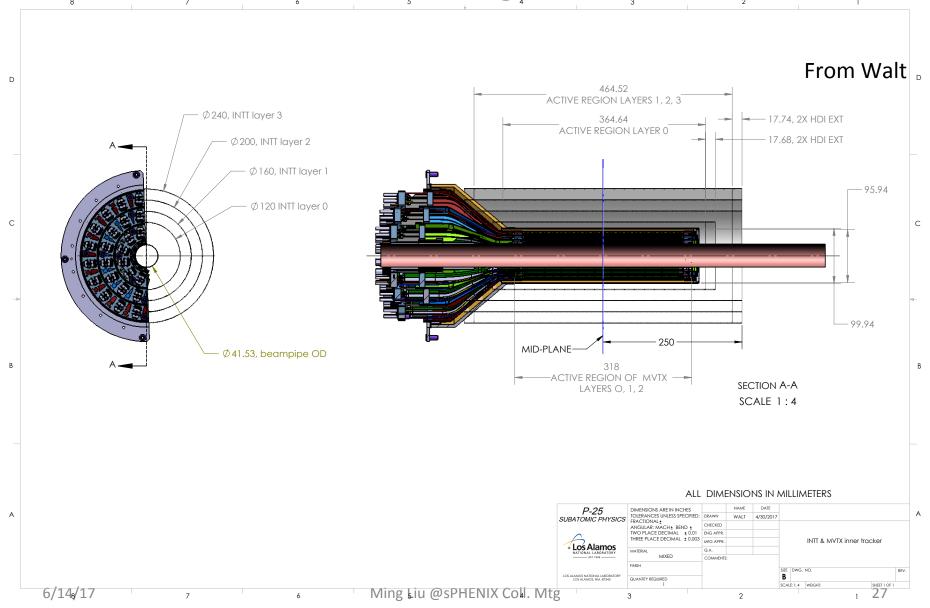
CCNU option \rightarrow plan A?

- Plan-B
 - HICs production @CCNU, Sep. 2018, 2-3 months
 - Stave space frame production @CERN ITS/IB, by 2017
 - Stave assembly: US/LBNL? Or China/CCNU, 4-6 months

Latest News from CERN

- 1) FPC and chip gluing has ben tested and settled. Production will use 90 microns droplet glue which introduced minimum material budget.
- 2) Production starts early July. One stave per day. Expect first ALICE/ITS ready January 2018, second detector ready in June 2018.
- 3) Confirmed MAPS chips and staves frames being produced for MVTX as part of the ALICE contingency
- 4) Despite the rumors propagated recently, the stave assembly room, machinery and personal will be available after ALICE production. They are also going to make a replica of the entire ITS for NIKA experiment in Dubna during 2019-2020. ATLAS consults on the possibility to use the MAPS technology for their inner tracker upgrade in the future. If they decide for it they will use a completely different facility.
- 5) LANL is going to send post-docs for 2-3 months stages at CRN to work on the stave characterization.
- 6) FZU Institution from Prague are also sending post-docs and staff to CERN to work on stave characterization.
- 7) We are discussing the possibility for Prague to send a skilled person to work on the construction of the staves. This task requires a skilled person, long training, and to stay at CERN at least six months.
- 8) Will have at least one stave sent to LANL for R&D in June. We expect to have four (at least partially functioning) staves by the end of September.

MVTX/INTT Integration Issues

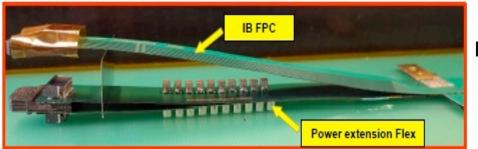


FPC Extension for Connection to Electrical Services

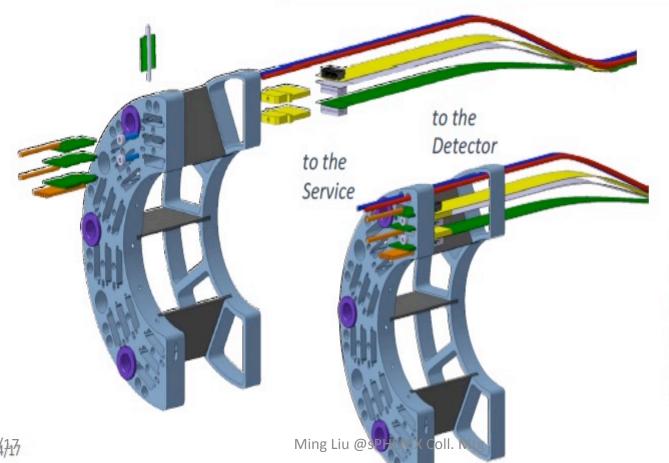
ALICE ITS Upgrade



Such extensions are equipped with passive components ($10x\ 220\ \mu F$ capacitors) to stabilize the analogue and digital power supplies, respectively



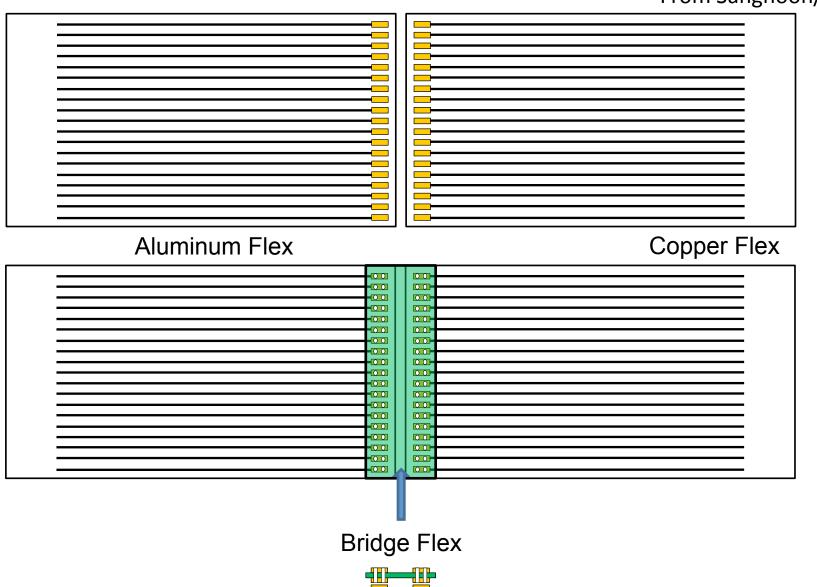
From Walt



This solution allows to implement a "flexible" connection to external service cables with minimized space occupancy

Possible Low Profile Connections

From Sanghoon/Walt



Summary and Outlook

- Exciting physics and great opportunity!
- A lot happened
 - Physics and detector simulations & optimization
 - Good progress with MAPS readout R&D
 - Mechanical integration
 - Some challenges due to delays in ALICE ITS R&
- A lot to do
 - Staves, RU, FELIX/CRU integration
 - PS and controls
 - BNL, DOE Reviews
 - Build and operate the detector
 - and more fun ...
 - Join us!

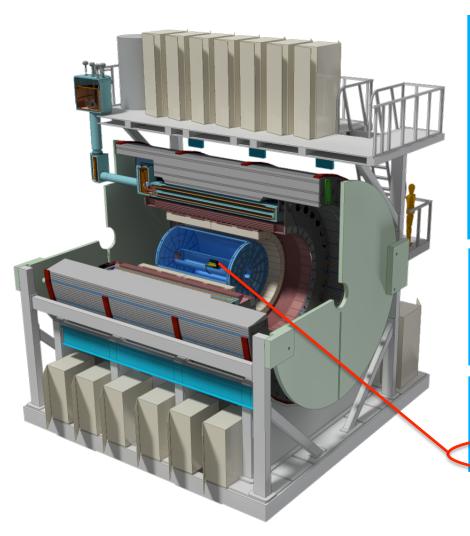


Winter Collaboration Meeting @Santa Fe A 2.5-day event

- Things to consider:
 - Before or after final exams, or winter breaks
 - Avoid other major meetings/reviews
 - Avoid busy travel seasons
 - Good time for sPHENIX planning etc.
- Possible dates (Fri-Sun?)
 - Nov. 17-19
 - Dec. 1-3
 - Dec. 8-10
 - Jan. 5 -7, 2018

backup

MVTX: WBS 1.12



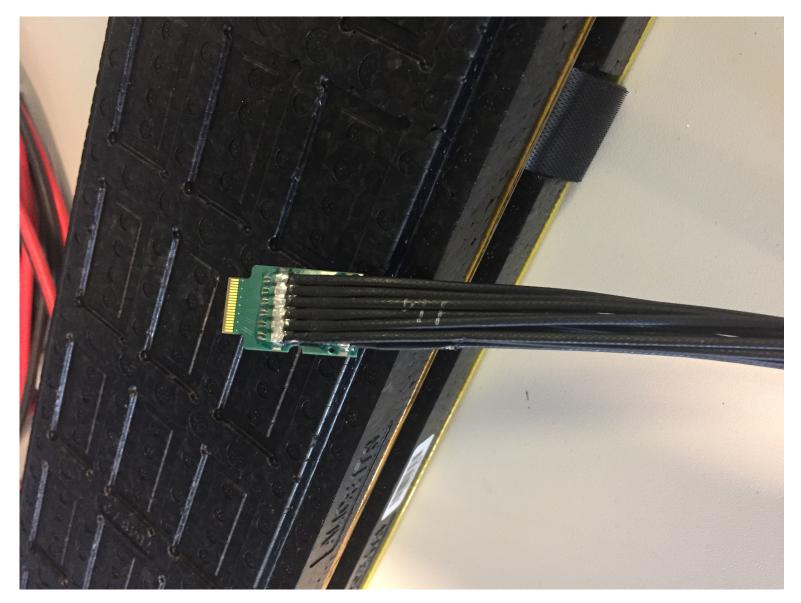
$\overline{ ext{WBS}}$	sPHENIX MIE Project Elements
1.1	Project Management
1.2	Time Projection Chamber
1.3	Electromagnetic Calorimeter
1.4	Hadron Calorimeter
1.5	Calorimeter Electronics
1.6	DAQ-Trigger
1.7	Minimum Bias Trigger Detector

WBS	Infrastructure & Facility Upgrade
1.8	SC-Magnet
1.9	Infrastructure
1.10	Installation-Integration

WBS	Parallel Activities
1.11	Intermediate Silicon Strip Tracker
1.12	Monolithic Active Pixel Sensors

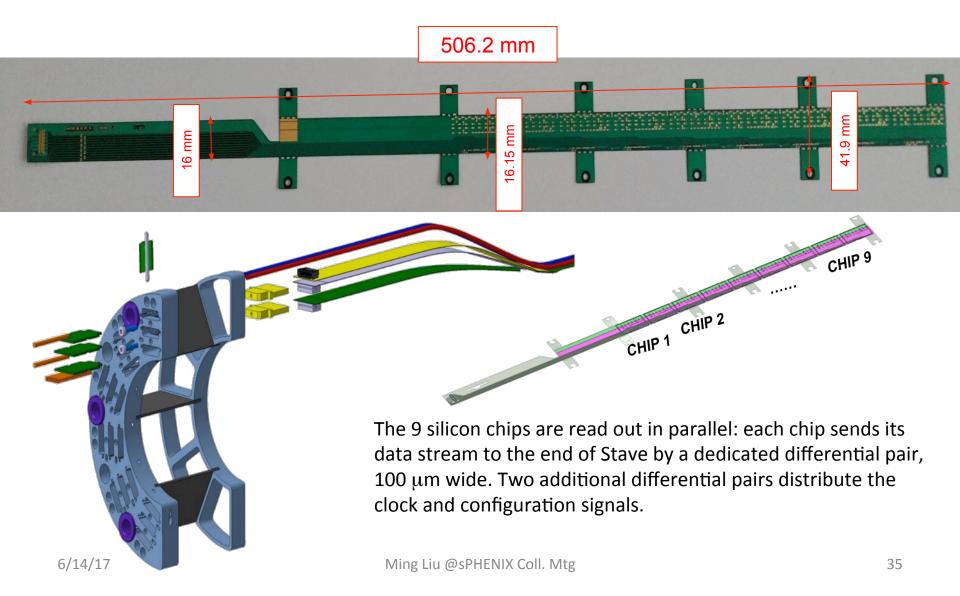
A separate MIE as an upgrade project

FPC and FireFly Cable Extension



MVTX/INTT Integration

Extend MVTX Service Cables?



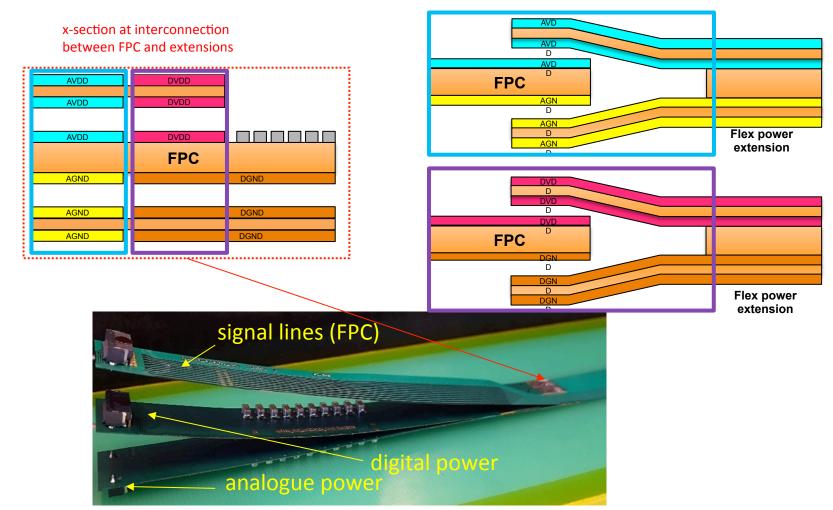
FPC Extension for Connection to Electrical Services





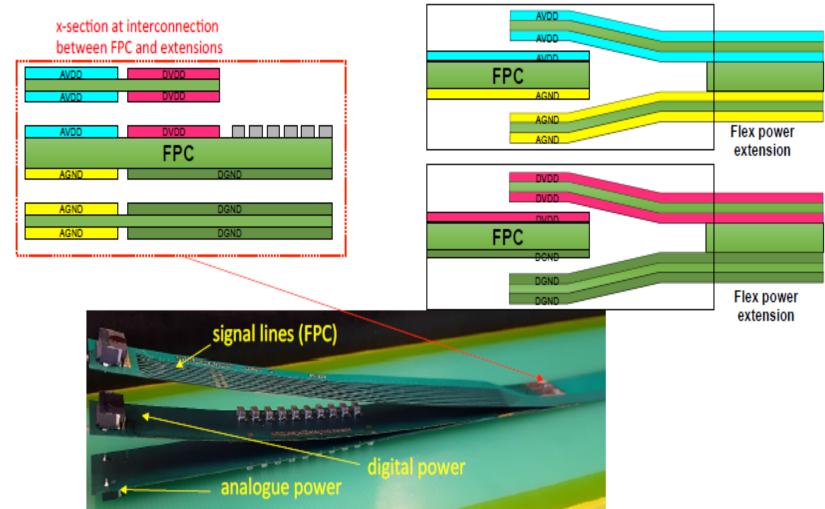
Antonello Di Mauro, Stave PRR 4/27/2017

The connection to the service cables is achieved by a double FPC extension which is soldered to the HIC

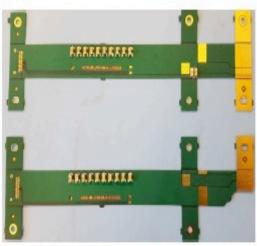


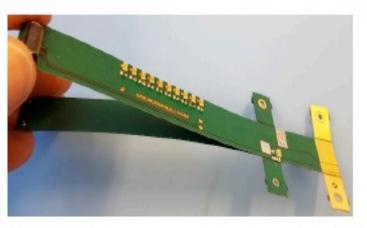


The connection to the service cables is achieved by a double FPC extension which is soldered to the HIC



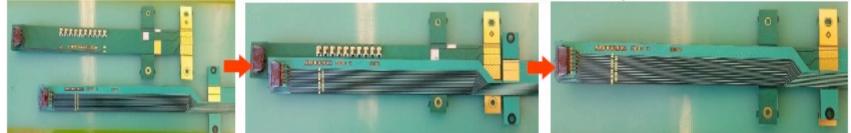






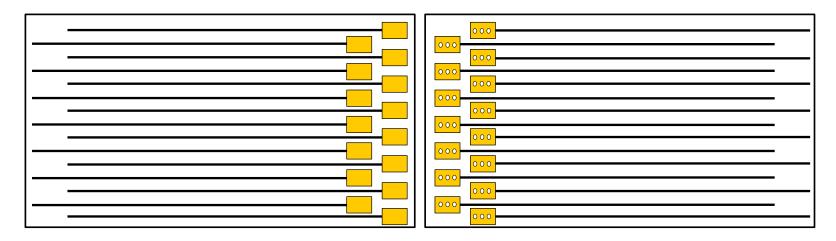
2 Cu layer flex, PI : 50 μm , Cu : 35 μm , Solder mask : 20 μm

The 2 flexes are glued together, in the middle to have a 4 layers flex.



The PWR_extension is connected to the FPC by iron soldering.





Aluminum Flex

Copper Flex



HICs Assembly Lab @CCNU

space ~ 70m² (1K clean room); 20m² (10K clean room, 2.9m head room)

- Chip and FPC gluing
- Gluing FPC/MAPS
- Chip mounting
- Wire Bonding
- Electrical circuit testing
- Storage

Machine shop: (Sun, Daming, Tech.)

- CNC etc.
- Simple mechanical structures

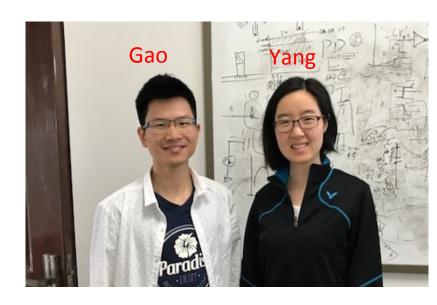
Not Doing at present:

- Stave assembly
- No carbon structures



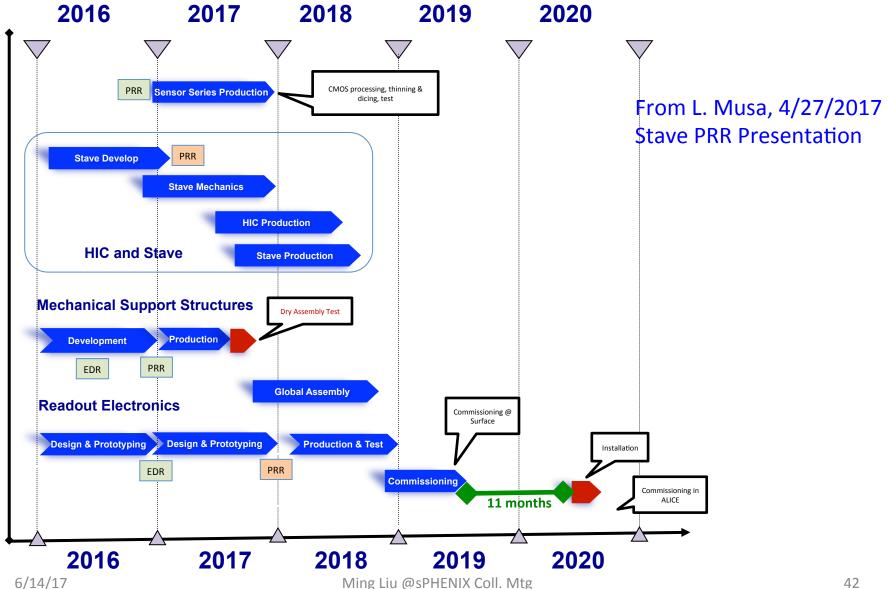
CCNU Plan - Cont.

- Experts and Designers of ALICE MAPS/ALPIDE on-chip electronics
 - Analogy circuit Dr. Chaosong Gao
 - Digital circuit Dr. Ping Yang
 - They will help us!
- PLAC Pixel Lab At CCNU
 - Also interested in mechanical system integration
 - Plan to hire a full time engineer to work on sPHENIX integration effort
 - Visit LANL 6-12 months, work on preliminary conceptual design for the MVTX/INTT/TPC
- Physics simulation and analysis
 - Many students











From L. Musa, 4/27/2017

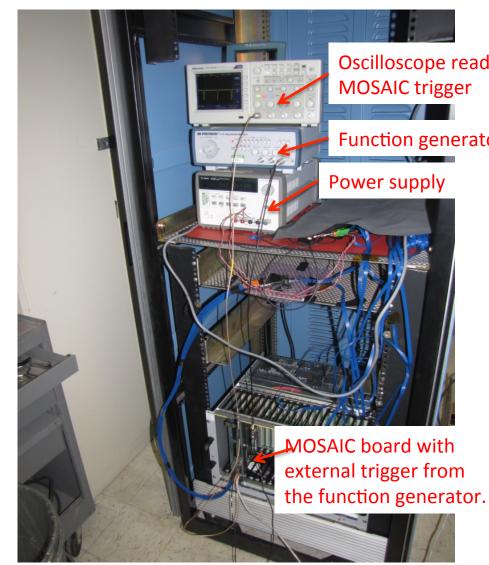
- Pixel Sensor Chip EDR (Oct' 15)
- 2 Stave EDR (May' 16)
- 3 Detector Barrel Mechanics EDR (Jul '16)
- 4 Cooling EDR (Jul '16)
- ⑤ Pixel Sensor Chip PRR (Nov '16)
- 6 Detector Barrel Mechanics PRR (Dec '16)
- Service Barrel Mechanics EDR (Dec '16): done
- (8) Cooling PRR (Dec '16): done
- Readout Electronics EDR (Jan '17): done
- 10 Stave PRR (Apr '17)
- Service Barrel Mechanics PRR (May '17)
- 12 Readout Electronics PRR (Dec '17)

Stave Production Readiness Review: 4/27/2017

- Stave production starts ~May/June;
- 1st set of IB by Jan 2018;
- 2nd set of IB by July 2018
- LANL people + others/MVTX work on stave production from May 2017 at CERN, prototype available soon at LANL
- Fully working staves for R&D available
 ~Jan 2018;
- Near final readout RU/CRU: ~12/2017

External trigger setting with a pulse generator

- Use Chip 4 for test.
- Use a pulse generator as the external trigger source. Now use 2MHz square pulse.
- Readout the FE trigger output of the MOSAIC board and check in the oscilloscope.
- Need to tune the external trigger to be in the phase locker.



Test under internal trigger (40MHz)

From Xuan

- Readout speed 600 Mb/s and 50 injections.
- Scan the threshold per pixel and the average value is 394.33±41.79 (e).

